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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/608,050

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Brent Stone

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7590

03/08/2005

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EXAMINER

TRAN, LONG K

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/608,050

Applicant(s)

STONE, BRENT

Examiner

Long K. Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 14-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 13 and 27 - 30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group I**, claims **1 – 13** and **27 - 30** in the reply filed on January 13, 2005 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1 – 5** and **7 – 13** are rejected under 35 U.S.C. 102(b) as being anticipated by Coico et al. (US Patent no. 6,354,844).

Regarding claim **1**, Coico et al. disclose an electronic package comprising:

Non-insertable feature 17 (figs 1 & 2) at a first surface of the electronic package;

and

Insertable feature 23 (fig. 1) extending perpendicularly from the first surface.

- Regarding claim **2**, Coico et al. disclose the electronic package comprises an IC 3 (figs. 1 & 2; col. 3, line 14).

Regarding claim **3**, Coico et al. disclose the non-insertable feature 17 (figs 1 & 2) include land grid array land (col. 3, lines 10 – 31).

Regarding claim **4**, Coico et al. disclose the insertable feature includes pin (col. 4, line 37).

Regarding claim **5**, Coico et al. disclose the insertable feature 23 (fig. 1) could be a low insertion force feature (col. 4, lines 55 – 63).

Regarding claim **7**, Coico et al. disclose non-insertable feature is couple to circuits that use or produce I/O signals (col. 3, lines 40 – 45; col. 4, lines 45 – 50 and col. 5, lines 61 +), and the insertable feature is electrically coupled to circuits that consume power or require ground connection (col. 4, lines 18 – 21).

Regarding claims **8** and **10**, Coico et al. disclose a receptacle 21, 25 (fig. 3. Note: the receptacle comprising an interposer 21 and circuit board 25 similar to he claimed invention) comprising:

Non-insertable contacts 19 (fig. 3) at a first surface of the receptacle; and

Insertable contacts 29 (fig. 3) having opening on the first surface,

Wherein the non-insertable contacts and the insertable contacts are arranged to make electrical contact with non-insertable features and insertable features of a single electronic circuit package brought in contact with the receptacle (col. 5, lines 1+).

Regarding claim **9**, Coico et al. disclose the receptacle comprises socket (col. 1, line 35) or alignment components including holes 29 with sleeves 33 (col. 5, lines 5 – 15).

Regarding claim **11**, Coico et al. disclose the non-insertable contact includes a land grid array contact (abstract and col. 3, lines 34 and 35).

Regarding claim **12**, Coico et al. disclose the insertable contact includes an alignment component 33 (fig. 1) to receive pin features 23 and 24 (fig. 1; col. 4, lines 22 – 29).

Regarding claim **13**, Coico et al. disclose the insertable contact includes a low insertion force contact (col. 4, lines 55 – 63).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al. (US Patent no. 6,354,844) in view of Liang (US Patent no. 5,532,612).

6. Regarding claim **6**, Coico et al. disclose the claimed invention of claim but fails to teach the feature count is greater than 400 features. However, the complexity and density of an IC have increased, therefore the number of I/O (feature counts) has also increase, 128 bit microprocessor may require 500 to 100 I/o terminals, as shown by Liang (c00l. 1, lines 22 – 40). It would have been well known in the art that the selection of those parameters such as **energy, number, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art.

"Normally, it is to be expected that a change in **energy, concentration,**

number, temperature, time, molar fraction, depth, thickness, etc., or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Moreover, the feature count has not been alleged by applicant to be of significant importance for patentability.

7. Claim **27 – 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al. (US Patent no. 6,354,844) in view of Kabadi et al. (US Patent Application Publication no. 2003/0168738).

8. Regarding claim **27**, Coico et al. disclose an electronic package 1 (figs 1 & 3) having non-insertable feature 17 (figs 1 & 3) at a first surface of the electronic package and Insertable feature 23 (fig. 1) extending perpendicularly from the first surface;

a receptacle 21, 25 (fig. 3. Note: the receptacle comprising an interposer 21 and circuit board 25 similar to he claimed invention) couple to the electronic package, and

having non-insertable contacts 19 (figs 1 & 3) and Insertable contacts 23, 24 (fig. 1) or 29 (fig. 3) wherein when the electronic circuit package is joined with the receptacle, the non-insertable contact makes conductive contact 19 (figs 1 & 3) with a non-insertable feature 17 (figs 1 & 3);

an IC 3 (figs 1 & 3) located on the electronic circuit package.

Coico et al. do not explicitly show the electronic circuit package and a display coupled to the electronic circuit package within an electronic system.

Although Coico et al. do not specify the electronic circuit package and a display coupled to the electronic circuit package within an electronic system. However, an electronic circuit package including electronic circuit, package, receptacle (interposer, socket) and printed circuit board is well known in the microelectronic art being used in the an electronic system with a display as an electronic system 270 (fig. 14; [0002]) including electronic assembly with socketable IC package 274 (fig. 14; [0008]) and display 279 (fig. 14; [0074]) as shown by Kabadi et al. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to integrate Coico et al. device into the electronic system as shown by Kabadi et al, since it has been held to be within the general skill of a worker in the art to select a known device on the basis of its suitability for the intended use.

Regarding claim **28**, Coico et al. disclose a device to apply a sustained, vertical, compressive force to increase a contact pressure between the non-insertable feature and the non- insertable contact (col. 4, lines 55 – 63 and col. 5, lines 26 - 37).

Regarding claim **29**, Coico et al. disclose a device to apply a sustained, normal force to increase a contact pressure between the insertable feature and the insertable contact (col. 4, lines 55 – 63 and col. 5, lines 26 - 37).

Regarding claim **30**, Kabadi et al. disclose the electronic system comprises a server system ([0002]).

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran 

March 2, 2005


David Nelms
Supervisory Patent Examiner
Technology Center 2800